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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/679,461	10/04/2000	Richard J. Ely	2494/103	5412

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/679,461	ELY ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32 and 34-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,15-21,31-37 and 46-48* is/are rejected.

7)☒ Claim(s) *6-14, 22-30, 38-45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed on 4/20/2005.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 4-5, 15, 17, 20-21, 31-32, 36-37 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fradette (US PAT. 6,606,698) in view of Isono et al. (US PAT. 5,892,918 hereinafter Isono).

Regarding claim 1, Fradette discloses a memory interface device (10, figure 2), i.e., data storage managing apparatus, for interfacing a number of host applications (30, figure 2) to a memory device (20, figure 2 and col. 3 lines 7-41), the memory interface device comprising a host interface (120, figure 4) for interfacing with number of host applications in a protocol associated with the corresponding host application (col. 3 line 49 through col. 4 line 12 and col. 6 lines 27-51), a memory interface (180, figure 6) for interfacing with the memory device wherein one or more of the host applications and the memory device operate in response to different protocols (col. 7 line 61 through col. 8 line 5), a number of contexts (124, figure 4) operably coupled to the host interface for receiving memory access requests from the number of host applications (col. 4 lines 18-30 and col. 7 lines 5-17), control logic (60, figure 3) operably coupled to obtain memory access requests from the number of host applications in a protocol associated with the corresponding host interface, translated the memory access requests into memory access requests in accordance with a protocol of the memory device, interact with the memory device over the memory interface for servicing the memory access requests on behalf of the number of host applications (col. 3 line 45 through col. 4 line 30 and col. 5 line 62 through col. 7 line 28). Fradette differs from the claimed invention in not specifically teaches the number of contexts for providing result/status information to the number of host applications, wherein at least one context is provided for each host application so that the control logic operably to provide the result/status information to the number of host applications via the number of contexts in accordance with the protocol associated with each of the number of host applications. However, Isono discloses a parallel computer system comprising a plurality of logical processing unit (20, figure 2), i.e., host applications, and a connecting device (10, figure 2) wherein the

connecting device comprising a list controls (41, figure 3) which each include a list number identifying the list in question, user information indicating which logical processing unit of the logical processing units, in addition, the connecting device further transmits commands or acknowledgements of the incoming commands from/to each of the logical processing units individually via the input/output processor (20-3, figure 4) of the processing unit, i.e., host interface, and the input/output processor (10-3, figure 4) of the connecting device (col. 5 line 41 through col. 6 line 54), furthermore, Isono discloses the connecting device further comprising a message command block (50, figure 4) wherein the message command block including command information of each of the logical processing unit, i.e., one context/information for each host application, (figures 7-8) and (col. 6 line 55 through col. 8 line 28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of Fradette in having a number of contexts for providing result/status information to the number of host applications, wherein at least one context is provided for each host application so that the control logic operably to provide the result/status information to the number of host applications via the number of contexts in accordance with the protocol associated with each of the number of host applications, as per teaching by the parallel computer system of Isono, because it reduces the number of commands exchanged between the processing unit and the connecting device and minimizing delays in command execution which are attributable to the increase in command traffic.

Regarding claim 4, Fradette discloses the number of contexts comprise a number of context registers sets (126, figure 4 and col. 4 lines 18-30 and col. 7 lines 5-17).

Regarding claim 5, Fradette discloses each context register set corresponds to one and only one of the number of host applications, i.e., each memory region (126, figure 4) in memory map (124, figure 4) is assigned to a separate interface module (120, figure 4) which corresponding to each host applications (col. col. 4 lines 18-30 and col. 7 lines 5- 17).

Regarding claim 15, Fradette discloses the memory interface device as programmed programmable logic device (10, figure 3 and col. 3 lines 2 1-30).

Regarding claim 17, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 20, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 21, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 31, the limitations of the claim are rejected as the same reasons set forth in claim 15.

Regarding claim 32, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 36, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 37, the limitations of the claim are rejected as the same reasons set forth in claim 15.

Regarding claim 47, the limitations of the claim are rejected as the same reasons set forth in claim 15.

4. Claims 2, 16, 18, 34 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fradette (US PAT. 6,606,698) in view of Isono et al. (US PAT. 5,892,918 hereinafter Isono) as applied to claims above, and further in view of Wentka et al. (US PAT. 5,968,114).

Regarding claim 2, the combination of Fradette and Isono differs from the claimed invention in not specifically teaches the number of host applications comprises a number of packet processing contexts of a packet processor, and wherein the host interface conforms to a packet processor interface. However, Wentka teaches the processing elements (12, figure 1) comprises separate processing elements (30, figure 1) and input/output processors (col. 5 lines 65- 67), wherein processor interface conforms to a packet processor interface (figure 2, and col. 4 lines 1-6). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of the combination of Fradette and Isono in having the host applications comprises a number of packet processing contexts of a packet processor, and wherein the host interface conforms to a packet processor interface, as per teaching of Wentka because it provides to communicate data with the CPU'S or processors utilizing the time division multiplexing.

Regarding claim 16, Wentka teaches the memory interface device as an application specific integrated circuit (col. 10 lines 23-28).

Regarding claim 18, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 34, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 48, the limitations of the claim are rejected as the same reasons set forth in claim 16.

5. Claims 3, 19 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fradette (US PAT. 6,606,698) in view of Isono et al. (US PAT. 5,892,918 hereinafter Isono) as applied to claims above, and further in view of Bauman et al. (US PAT. 5,875,472 hereinafter Bauman).

Regarding claim 3, the combination of Fradette and Isono differs from the claimed invention in not specifically teaches the memory device comprises a content-addressable memory, and wherein the memory interface conforms to a content-addressable memory However, Bauman teaches in a multiple processing system comprising a memory interface device (28, figure 2A) for interfacing a number of host applications (31, 33, 35 and 37, figure 2A) to a memory device (54, figure 2A), the memory interface device comprising a host interface for interfacing with the number of host applications (col. 7 lines 62-64), a memory interface for interfacing with the memory device (col. 9 lines 43-47), and the memory interface further comprising an associated global second-level cache labeled 50 wherein each is capable to the a1 of system's addressable memory included in shared main memory (col. 8 lines 3-11 and col. 8 line 57 through col. 9 line 29). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the storage device of the combination of Fradette and Isono being a content-addressable memory, and wherein the memory interface conforms to a content-addressable memory, as per teaching of the computer

system of Bauman, because it improves address conflict detection and resolution system for a multiple processor data processing system.

Regarding claim 19, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claim 35, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Allowable Subject Matter

6. Claims 6-14, 22-30 and 38-45 arte objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on M-F 9:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

Patent Examiner
Art Unit 2189

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